

# CBCS SCHEME

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17EC53

## Fifth Semester B.E. Degree Examination, Jan./Feb.2021

### Verilog HDL

Time: 3 hrs.

Max. Marks: 100

**Note: Answer any FIVE full questions, choosing ONE full question from each module.**

#### Module-1

- 1 a. Explain the typical design flow for designing VLSI IC circuits with neat block diagram. (10 Marks)  
b. Explain the Top down and Bottom up design methodology with an suitable example. (10 Marks)

OR

- 2 a. Explain the following components in a simulation (i) Design block (ii) Stimulus block. (06 Marks)  
b. Make use of T-Flip Flop build a 4-bit Ripple carry counter and explain the design hierarchy. (10 Marks)  
c. Explain the Trends in HDLs. (04 Marks)

#### Module-2

- 3 a. List all the lexical convention used in verilog and explain with examples. (08 Marks)  
b. Explain the two methods of connecting ports to external signal with an example. (08 Marks)  
c. Explain the compiler directives in verilog HDL. (04 Marks)

OR

- 4 a. What are the data types in verilog? Explain the following data types with suitable example:  
(i) Nets (ii) Parameter (iii) Array (iv) Memory (08 Marks)  
b. Write the Verilog code for SR Latch using gate level mode and also write stimulus code. (06 Marks)  
c. With neat block diagram, explain the components of verilog module. (06 Marks)

#### Module-3

- 5 a. Explain the following gate primitives used in verilog HDL with truth table:  
(i) Bufif (ii) notif (04 Marks)  
b. Construct a 4-bit Ripple carry adder and develop the verilog code using gate level model, also write stimulus code. (08 Marks)  
c. What should be the output of the following:  $A = 4'd_{10}$ ,  $B = 4'd_{13}$ ,  $C = 4'b_{|0x|}$ .  
(i)  $A \wedge B$  (ii)  $|B$  (iii)  $B \gg 2$  (iv)  $A \gg \gg 2$  (v)  $Y = \{3\{A\}, 2\{B\}\}$   
(vi)  $Y = \{A[2:0], B[3:1]\}$  (vii)  $A \& C$  (viii)  $A \parallel B$  (08 Marks)

OR

- 6 a. Construct a 4-bit carry look ahead adder and develop the verilog code using data flow description. (08 Marks)  
b. Write the verilog code for 4 to 1 multiplexer using conditional operator. (06 Marks)  
c. What are Rise, Fall and Turnoff delays? How they are specified in verilog? (06 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice.

**Module-4**

- 7 a. Explain the blocking and non blocking assignment statements with suitable example. (06 Marks)
- b. What are the different delay based timing controls are associated with verilog HDL and explain with relevant example. (08 Marks)
- c. Using case statement, design an 8-function ALU that takes 4-bit inputs 'a' and b and a 3-bit input signal select 1, and gives a 5-bit output 'out'. The ALU implements the following functions based on a 3 bit input signal select. Ignore any overflow or underflow bits.

Select signal	3'd <sub>0</sub>	3'd <sub>1</sub>	3'd <sub>2</sub>	3'd <sub>3</sub>	3'd <sub>4</sub>	3'd <sub>5</sub>	3'd <sub>6</sub>	3'd <sub>7</sub>
Function (out)	a	a + b	a - b	a / b	a % b	a << 1	a >> 1	a > b

(06 Marks)

**OR**

- 8 a. Explain the sequential and parallel blocks with suitable example. (08 Marks)
- b. Write a verilog code for 4 to 2 priority encoder using casex. (04 Marks)
- c. List the loop statements in verilog. Explain the following loops with examples:  
 (i) For loop (ii) Repeat (08 Marks)

**Module-5**

- 9 a. Compare VHDL and Verilog HDL. (04 Marks)
- b. Explain the synthesis process with a neat block diagram. (08 Marks)
- c. Explain the relationship between a design entity and its entity declaration and architecture body in VHDL? (08 Marks)

**OR**

- 10 a. Explain the following Data Objects in VHDL with examples :  
 (i) Constant (ii) Signals (iii) Variables. (09 Marks)
- b. What are the data types in VHDL? Explain the Scalar data types with examples. (07 Marks)
- c. Write the VHDL code for a 4-bit wide register ensure that the input DATA [3 : 0] is stored only when the 'CLOCK' signal is detected on its rising edge. (04 Marks)

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